Digital Logic Design Laboratory

Lab 5

Demultiplexers

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Class: ……………………………………………….......

Date: …………………………………………………....

# I. Objectives

In this laboratory, students will study:

- Understand and design a multiplexer.

- Use a demultiplexer and design/implement a circuit based on a function definition.

- Design combinational circuits using DEMUX.

# II. Procedure

1. Design demultiplexer using logic gates

a. Design 1-to-2 demultiplexer using logic gates:

A 1-to-2 demultiplexer has I is the input, S is the selector input, and Y1 and Y2 are two outputs. When S = 0 then Y0 = I but when S = 1 then Y1 = I. The Figure 1 shows the illustration of DEMUX 1-2.

Diagram, schematic

Description automatically generated

Figure 1. The illustration of DEMUX 1-2.

Built the truth table:

|  |  |  |  |
| --- | --- | --- | --- |
| Input | | Output | |
| S | I | Y0 | Y1 |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 |

The expressions:

Implement the circuit via simulation software and paste the result in here

A diagram of a circuit

Description automatically generated

A diagram of a circuit

Description automatically generated

Make comment on the results

When we build a circuit by using logic gates to replace the DEMUX 1-2 the output is rely on the input S and the output is rely on the input I

b. Design 1-to-4 DEMUX using logic gates.

Build the circuit. The inputs S0, S1, I, are driven by 3 switches. The outputs Y0, Y1, Y2, Y3 are connected to LED.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| q | | | Output | | | |
| S1­ | S0 | I | Y0 | Y1 | Y2 | Y3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

The expressions:

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a diagram

Description automatically generated

A screenshot of a computer

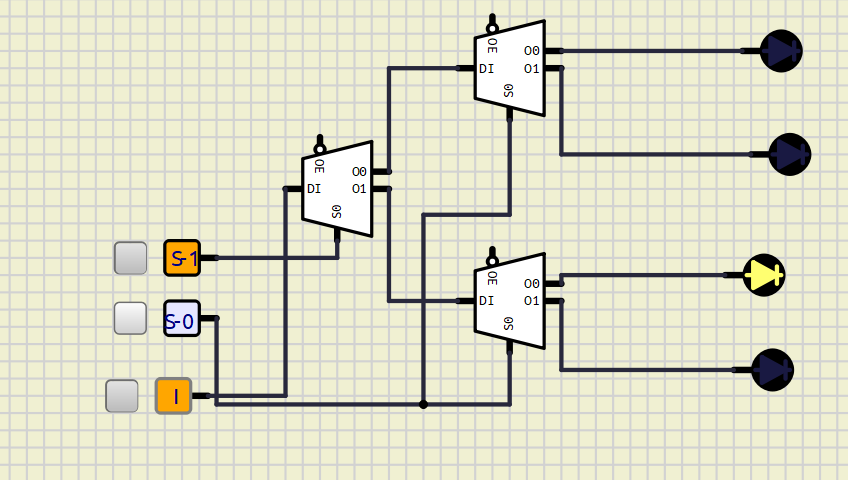
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Make comment on the results

The truth table represents a 1-to-4 demultiplexer, where S1 and S0 are the select lines that determine which output Y0 ,Y1, Y2, Y3 the input I is routed to. When I=1 the selected output is set to 1 while all others remain 0. When I =0 all outputs are 0 regardless of the select lines' values.

c. Design 1-to-4 DEMUX using 3 DEMUX 1-2.

Implement the circuit via simulation software and paste the result in here



A diagram of a computer

Description automatically generated

Make comment on the results

2. Investigate IC 1-to-8 DeMultiplexer (74HC238)

Construct the circuit as below:

Diagram, schematic

Description automatically generated

Figure 2. IC 1-to-8 DeMultiplexer (74HC238)

- 8 outputs are connected by using LEDs.

- The inputs are controlled by switches.

- Observe the results and fulfill the truth table

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| INPUT | | | OUTPUT | | | | | | | |
| S2 | S1 | S0 | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Implement the circuit via simulation software and paste the result in here

A computer screen shot of a circuit board

Description automatically generated

Briefly describe the operation of the IC

The truth table represents a 1-to-8 demultiplexer, where S2,S1 and S0 are the select lines that determine which output Y0 to Y7 is set to 1. For each combination of S2, S1, and S0, only one specific output is 1 while the others are 0. This setup channels a single input signal to one of eight outputs based on the select line values.

3. Design 1-bit Full Subtractor

a. Using logic gates

Construct the circuit as below:

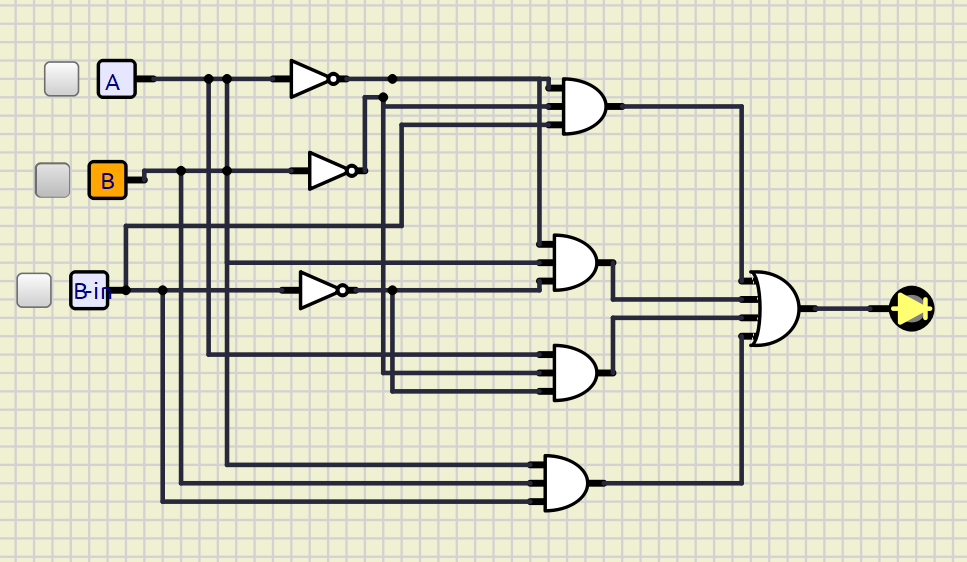
Three inputs are A, B, Bin. Two outputs are D and Bout.

Build the truth table and the expressions

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input | | | Output | |
| A | B | Bin | D | Bout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

The simplified expressions:

Implement the circuit via simulation software and paste the result in here



A diagram of a circuit

Description automatically generated

A diagram of a circuit

Description automatically generated

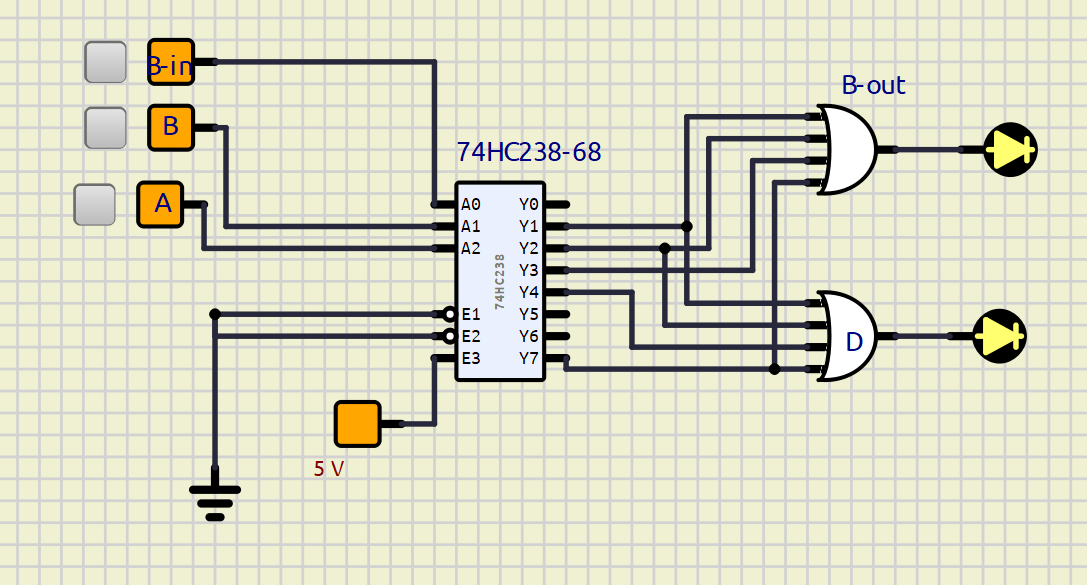
A diagram of a circuit

Description automatically generated

Make comment on the results

b. 1-to-8 DeMultiplexer (74HC238)

Implement the circuit via simulation software and paste the result in here



A computer diagram of a circuit board

Description automatically generated

Make comment on the results

4. Design 4-bit Full Adder using 74HC283 and display to BCD Seg

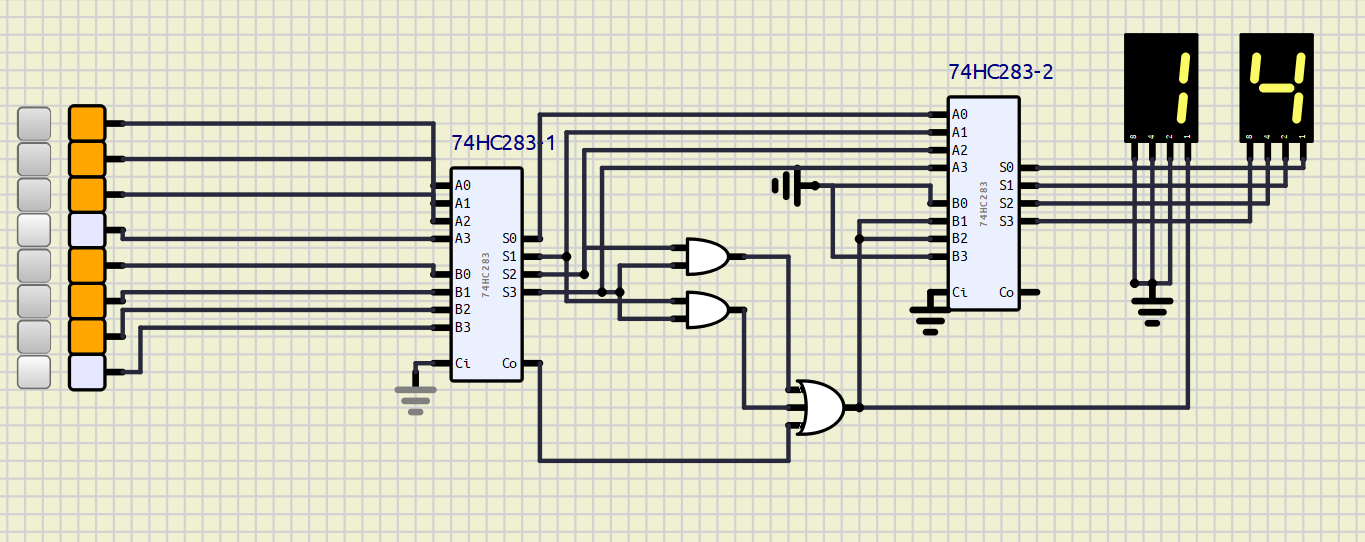
Construct the circuit as below:

Four inputs for A(A3, A2, A1, A0) and B(B3, B2, B1, B0). The outputs are display by BCD 7seg

Diagram

Description automatically generated

Implement the circuit via simulation software and paste the result in here



Make comment on the results

The maximum result is 19